

# 1-Mbit (128K x 8) Static RAM

## Features

- Pin- and function-compatible with CY7C1018CV33
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low Active Power
  - $I_{CC} = 60 \text{ mA @ } 10 \text{ ns}$
- Low CMOS Standby Power
  - $I_{SB2} = 3 \text{ mA}$
- 2.0V Data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Center power/ground pinout
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- Available in Pb-free 32-pin 300-Mil wide Molded SOJ

## Functional Description<sup>[1]</sup>

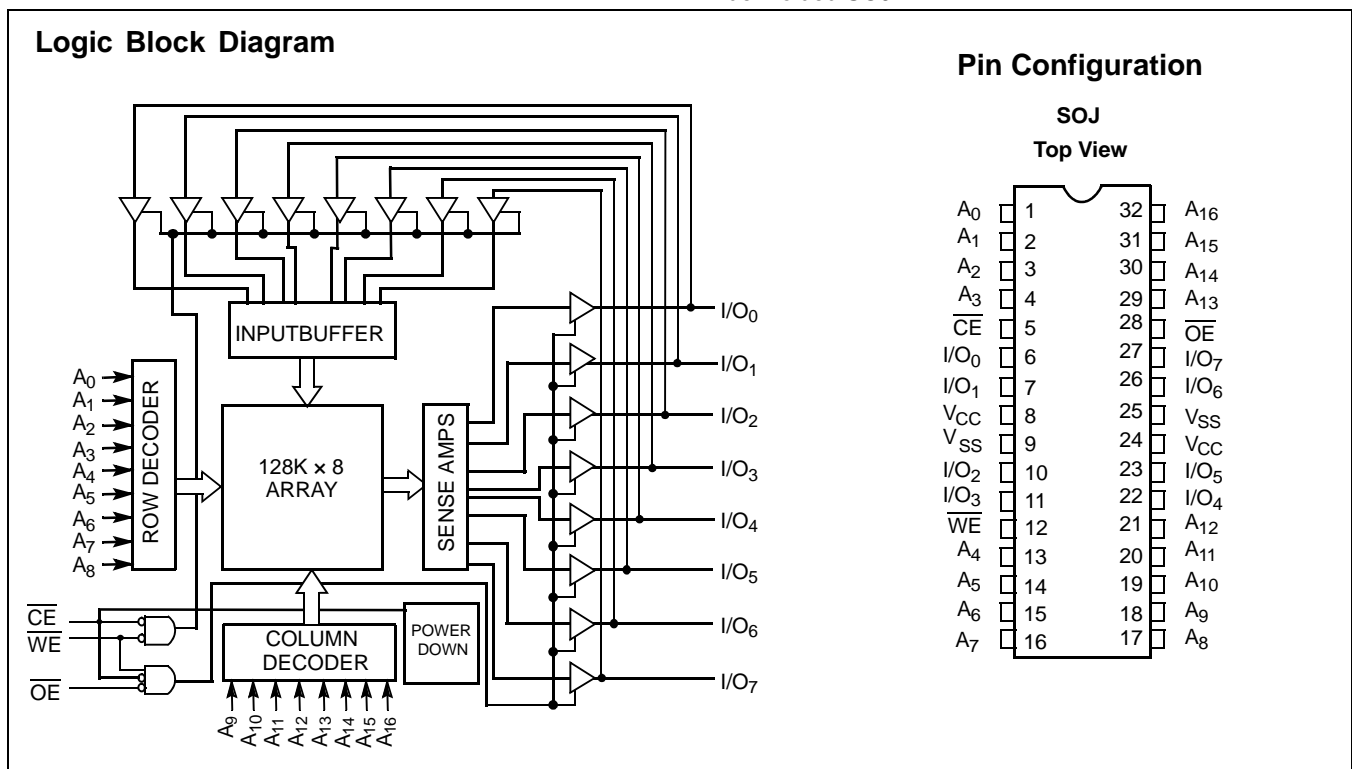
The CY7C1018DV33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1018DV33 is available in Pb-free 32-pin 300-Mil wide Molded SOJ.



### Note

1. For guidelines on SRAM system designs, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

**Selection Guide**

	<b>-10 (Industrial)</b>	<b>Unit</b>
Maximum Access Time	10	ns
Maximum Operating Current	60	mA
Maximum Standby Current	3	mA

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[2]</sup> ... -0.3V to + 4.6V  
 DC Voltage Applied to Outputs<sup>[2]</sup> in High-Z State ..... -0.3V to V<sub>CC</sub> + 0.3V

DC Input Voltage<sup>[2]</sup> ..... -0.3V to V<sub>CC</sub> + 0.3V  
 Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)  
 Latch-up Current ..... > 200 mA

**Operating Range**

<b>Range</b>	<b>Ambient Temperature</b>	<b>V<sub>CC</sub></b>	<b>Speed</b>
Industrial	-40°C to +85°C	3.3V ± 0.3V	10 ns

**DC Electrical Characteristics** Over the Operating Range

<b>Parameter</b>	<b>Description</b>	<b>Test Conditions</b>	<b>-10 (Industrial)</b>		<b>Unit</b>
			<b>Min.</b>	<b>Max.</b>	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	100MHz	60	mA
			83MHz	55	mA
			66MHz	45	mA
			40MHz	30	mA
I <sub>SB1</sub>	Automatic CE Power-down Current—TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		10	mA
I <sub>SB2</sub>	Automatic CE Power-down Current—CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		3	mA

**Note**

2. V<sub>IL</sub> (min.) = -2.0V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 1V for pulse durations of less than 5 ns.

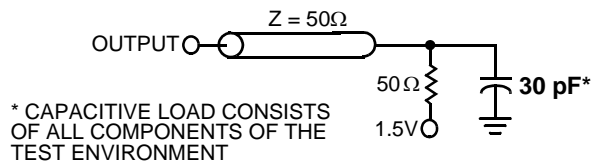
**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3V	8	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

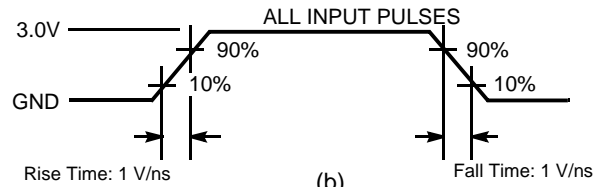
**Thermal Resistance<sup>[3]</sup>**

Parameter	Description	Test Conditions	400-Mil Wide SOJ	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.61	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		40.53	°C/W

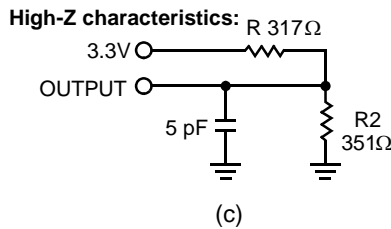
**AC Test Loads and Waveforms<sup>[4]</sup>**



(a)



(b)



(c)

**Notes**

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

**AC Switching Characteristics** Over the Operating Range <sup>[5]</sup>

Parameter	Description	-10 (Industrial)		Unit
		Min.	Max.	
<b>Read Cycle</b>				
$t_{\text{power}}^{[6]}$	$V_{\text{CC}}$ (typical) to the first access	100		$\mu\text{s}$
$t_{\text{RC}}$	Read Cycle Time	10		ns
$t_{\text{AA}}$	Address to Data Valid		10	ns
$t_{\text{OHA}}$	Data Hold from Address Change	3		ns
$t_{\text{ACE}}$	$\overline{\text{CE}}$ LOW to Data Valid		10	ns
$t_{\text{DOE}}$	$\overline{\text{OE}}$ LOW to Data Valid		5	ns
$t_{\text{LZOE}}$	$\overline{\text{OE}}$ LOW to Low-Z	0		ns
$t_{\text{HZOE}}$	$\overline{\text{OE}}$ HIGH to High-Z <sup>[7, 8]</sup>		5	ns
$t_{\text{LZCE}}$	$\overline{\text{CE}}$ LOW to Low-Z <sup>[8]</sup>	3		ns
$t_{\text{HZCE}}$	$\overline{\text{CE}}$ HIGH to High-Z <sup>[7, 8]</sup>		5	ns
$t_{\text{PU}}^{[9]}$	$\overline{\text{CE}}$ LOW to Power-up	0		ns
$t_{\text{PD}}^{[9]}$	$\overline{\text{CE}}$ HIGH to Power-down		10	ns
<b>Write Cycle<sup>[10, 11]</sup></b>				
$t_{\text{WC}}$	Write Cycle Time	10		ns
$t_{\text{SCE}}$	$\overline{\text{CE}}$ LOW to Write End	8		ns
$t_{\text{AW}}$	Address Set-up to Write End	8		ns
$t_{\text{HA}}$	Address Hold from Write End	0		ns
$t_{\text{SA}}$	Address Set-up to Write Start	0		ns
$t_{\text{PWE}}$	$\overline{\text{WE}}$ Pulse Width	7		ns
$t_{\text{SD}}$	Data Set-up to Write End	5		ns
$t_{\text{HD}}$	Data Hold from Write End	0		ns
$t_{\text{LZWE}}$	$\overline{\text{WE}}$ HIGH to Low-Z <sup>[8]</sup>	3		ns
$t_{\text{HZWE}}$	$\overline{\text{WE}}$ LOW to High-Z <sup>[7, 8]</sup>		5	ns

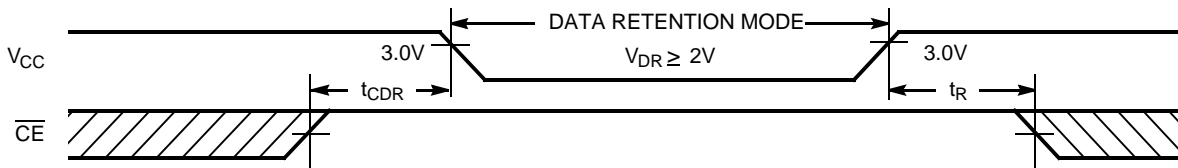
**Notes**

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
6.  $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at typical  $V_{\text{CC}}$  values until the first memory access can be performed.
7.  $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in (c) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
8. At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.
9. This parameter is guaranteed by design and is not tested.
10. The internal Write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
11. The minimum Write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

**Data Retention Characteristics** (Over the Operating Range)

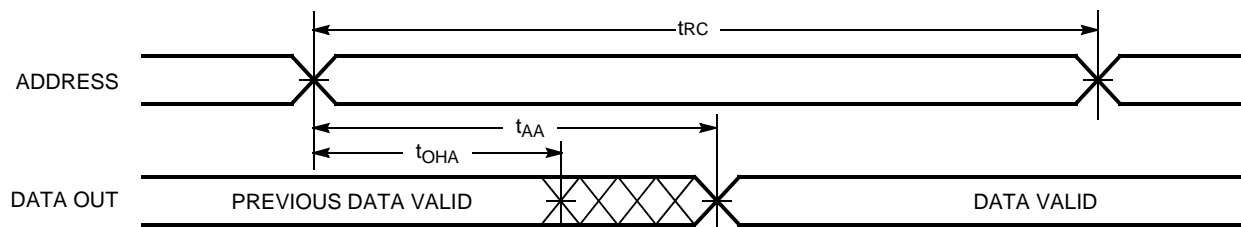
Parameter	Description	Conditions	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2		V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0V, \overline{CE} \geq V_{CC} - 0.3V, V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		3	mA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[12]}$	Operation Recovery Time		$t_{RC}$		ns

**Data Retention Waveform**

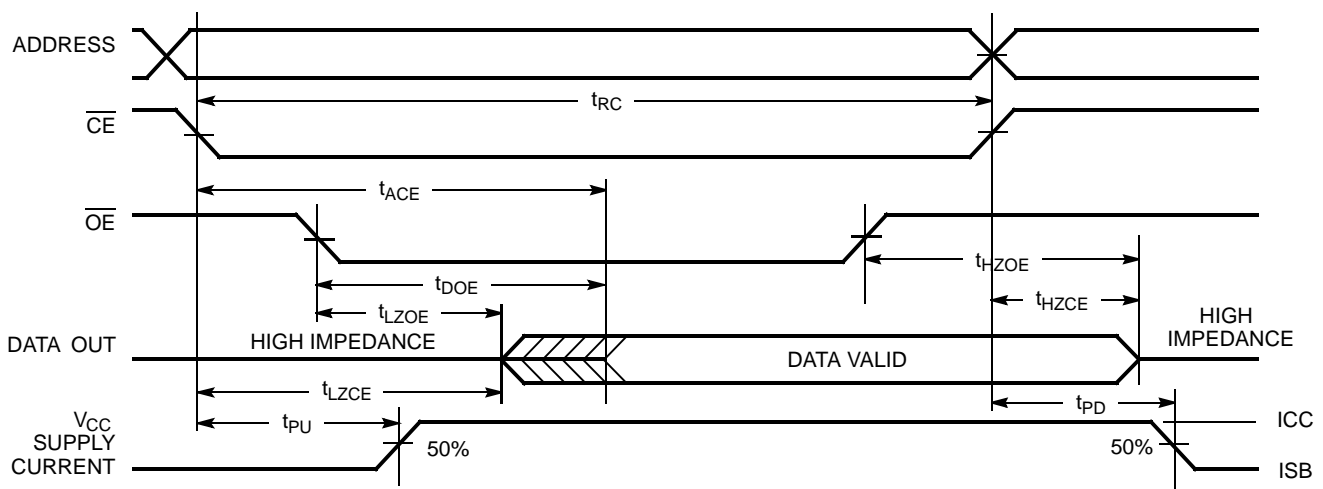


**Switching Waveforms**

**Read Cycle No. 1 (Address Transition Controlled)<sup>[13, 14]</sup>**



**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[14, 15]</sup>**

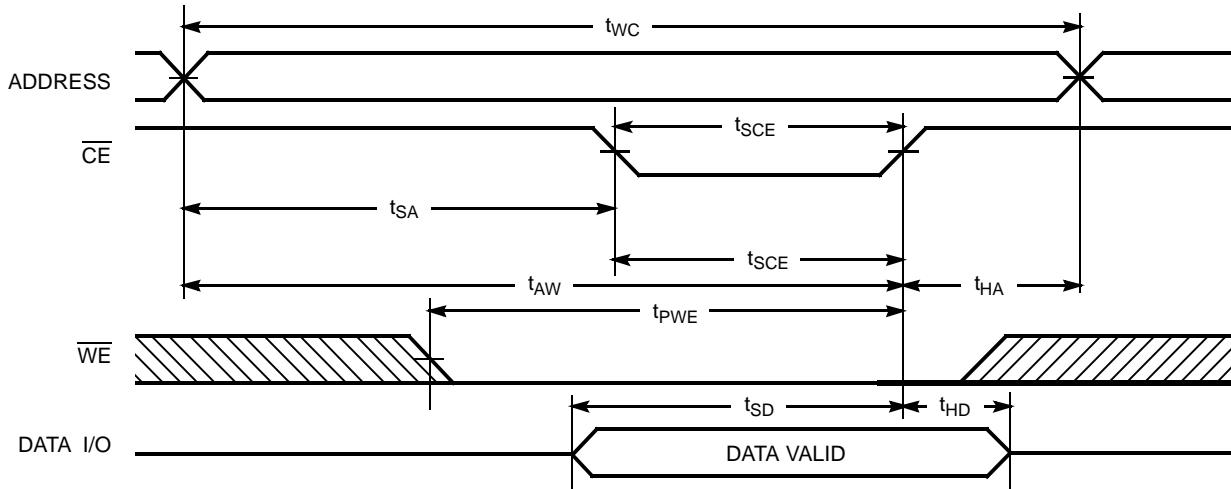


**Notes**

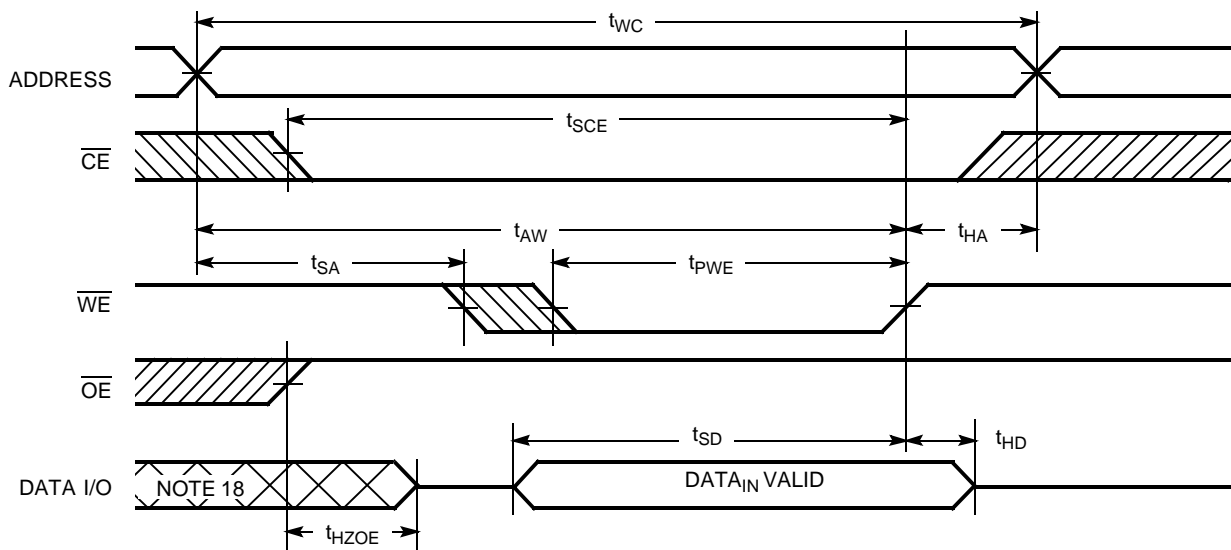
- 12. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50 \mu s$  or stable at  $V_{CC(min.)} \geq 50 \mu s$ .
- 13. Device is continuously selected.  $OE, CE = V_{IL}$ .
- 14.  $WE$  is HIGH for Read cycle.
- 15. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[16, 17]</sup>



Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[16, 17]</sup>

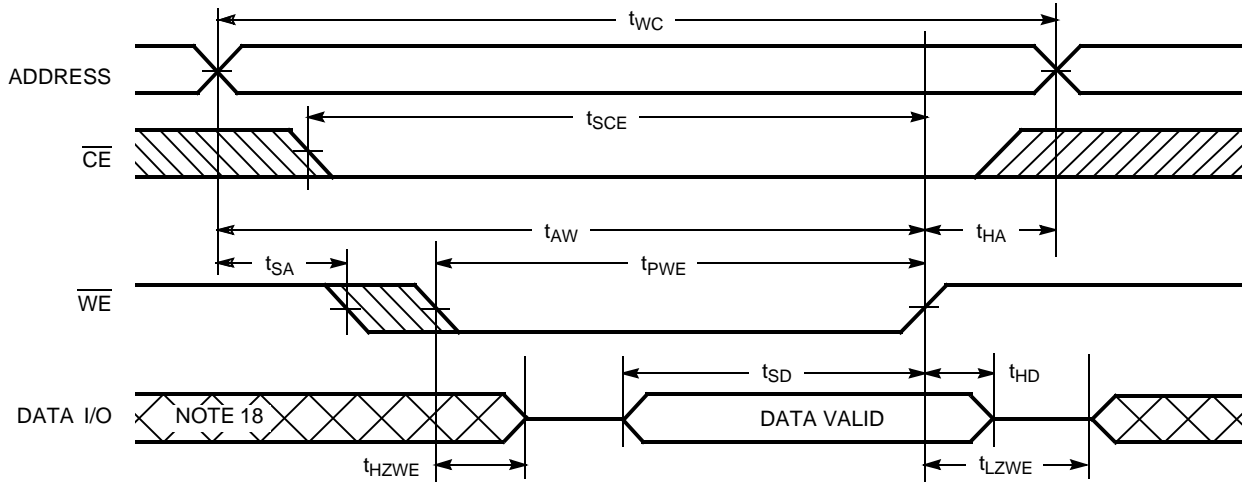


Notes

- 16. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 17. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 18. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[11, 17]</sup>**



**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	High-Z	Power-down	Standby ( $I_{SB}$ )
L	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High-Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1018DV33-10VXI	51-85041	32-pin (300-Mil) Molded SOJ (Pb-free)	Industrial

Please contact your local Cypress sales representative for availability of these parts.





Document History Page

Document Title: CY7C1018DV33, 1-Mbit (128K x 8) Static RAM				
Document Number: 38-05465				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	238471	See ECN	RKF	DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in the Ordering Information
*B	262950	See ECN	RKF	Added Data Retention Characteristics table Added T <sub>power</sub> Spec in Switching Characteristics table Shaded Ordering Information
*C	307598	See ECN	RKF	Reduced Speed bins to -8 and -10 ns
*D	520647	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 8 ns speed bin Added I <sub>CC</sub> values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V <sub>CC</sub> +2V to V <sub>CC</sub> +1V in footnote #2